Lecture 4 Summary

This lecture focused on Amdahl’s law in the multicore era. First, for the corollary for multicore chip cost, 2 assumption are made in this article: 1. A multicore chip of given size and technology generation can have at most n base core equivalents (BCE); 2. Architects have techniques for using the resources of multiple BCEs to create a core with better sequential performance (perf(r), and here we assumed that perf(r) = sqrt(r)).

As a reference, Amdahl’s law for the case of using n cores in parallel is:

, where f is fraction of a program’s execution time was infinitely parallelizable.

Here, the article mentions 3 different structure to discuss with: symmetric multicore chip, asymmetric multicore chip and dynamic multicore chip.

First, the article discusses about symmetric multicore chip. Suppose that there is a total resource budget of n and the BCE resources of r was devoted to increase each core’s performance, then there are n/r cores because that every core has the same resource. And each core has sequential performance of perf(r). Therefore, the Speedup equation becomes:

By this equation, some results can be gotten: 1. Increase f becomes critical for symmetric multicore chip to achieve best speedup. 2. Using more BCEs per core can still be optimal, although it is pretty small. 3. Moving to denser chip increases the performance overall.

Second, the article discusses about asymmetric multicore chip. Suppose that the largest core in the chip uses r resources and leave n-r resources for the one-BCE cores, then there are at most 1+n-r cores in a single chip, with perf(1) = 1. Therefore, the speedup equation becomes:

By this equation, there are two results: 1. Asymmetric multicore chip can have better and no worse performance than symmetric multicore chips. 2. Like symmetric multicore chips, denser multicore chips increase both speedup benefit and the optimal performance of the single core but much better.

Lastly, the article discusses about dynamic multicore chips. Suppose that the chip can dynamically combining up to r cores to boost performance of only sequential work and in parallel mode, the chip gets performance from all r 1-BCE cores in parallel. Then, the speedup equation becomes:

By this equation, we can know that dynamic multicore chips can offer best speedup than any one of the chips mentioned before.

However, this model is almost simplest one and many of the techniques are still not be developed. Therefore, there is still much to do.